

What is claimed is:

1           1.    An apparatus, comprising:  
2                a storage device to store data; and  
3                a block to adjust the position of the data in the  
4 storage device to account for at least one sampling error.

1           2.    The apparatus of claim 1, wherein the block  
2 adjusts a portion of the data in response to receiving a  
3 plurality of bits in response to sampling a portion of an  
4 incoming data.

1           3.    The apparatus of claim 1, wherein the block  
2 comprises a detector to detect the at least one sampling  
3 error.

1           4.    The apparatus of claim 3, comprising a counter  
2 block to provide a clock substantially synchronous with the  
3 data in response to detecting the at least one sampling  
4 error.

1           5.    The apparatus of claim 1, wherein the block  
2 comprises a sampling block to sample incoming data using a  
3 plurality of sampling clocks to provide a plurality of  
4 samples.





1        18. The apparatus of claim 10, further comprising a  
2 multiplexer to receive the plurality of samples and provide  
3 desirable sample from the plurality of samples to the  
4 storage device based on a control signal from the detector  
5 block.

1        19. An apparatus, comprising:  
2                a clock block to generate a plurality of sampling  
3 clocks;  
4                a sampling block to sample data using the  
5 plurality of sampling clocks to generate a plurality of  
6 sample values;  
7                a detector block to detect at least one sample  
8 irregularity based on the plurality of sample values; and  
9                a shift register to receive at least one of the  
10 plurality of sample values and to shift the at least one of  
11 the plurality of sample values in response to detecting the  
12 at least one sample irregularity.

1        20. The apparatus of claim 19, wherein the detector  
2 is an edge detector.

1        21. The apparatus of claim 19, wherein the shift  
2 register is a variable shift register.

1        22. A method comprising:  
2            storing data into a storage device; and  
3            adjusting the location of the data in the storage  
4 device to account for synchronization errors.

1        23. The method of claim 22, further comprising  
2 sampling incoming data to provide a plurality of samples.

1        24. The method of claim 23, further comprising  
2 detecting at least one sampling error in the plurality of  
3 samples.

1        25. The method of claim 24, further selecting a  
2 desirable sample from the plurality of samples and storing  
3 the desirable sample in the storage device.

1        26. The method of claim 22, wherein sampling the  
2 incoming data comprises sampling the incoming data at a  
3 rate at least three times faster than the rate of the  
4 incoming data.

1        27. The method of claim 22, wherein adjusting the  
2 location comprises shifting the data by two location in the  
3 storage device to account for sampling frequency being  
4 slower than a rate of an incoming data.

1        28. The apparatus of claim 22, wherein adjusting the  
2 location comprises not shifting the data in the storage  
3 device to account for sampling frequency being faster than  
4 a rate of an incoming data.

1        29. A system, comprising:  
2            a first control unit to transmit data; and  
3            a receiver to receive the data, the receiver  
4 comprising:  
5            a storage device to store data; and  
6            a control block to adjust position of the  
7 data in the storage device to account for at least one  
8 synchronization mismatch.

1        30. The system of claim 29, wherein the first control  
2 unit is a bridge of the system.